

**AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

**Claims 1-7 (Canceled).**

**Claim 8 (Previously Presented):** A semiconductor device according to claim 9, further comprising:

a second interlayer insulating film formed on the first intra-layer insulating film, the first pad and the wiring, the second interlayer insulating film being formed with at least one via hole, the via hole being disposed partially superposing upon the first pad as viewed along a direction parallel to a substrate normal; and

a second pad formed on the second interlayer insulating film, the second pad being connected to the first pad via a region in the via hole.

**Claim 9 (Previously Presented):**

A semiconductor device comprising:

a semiconductor substrate;

a first interlayer insulating film made of insulating material and formed on the semiconductor

**Preliminary Amendment filed June 8, 2007  
U.S. Patent Application Serial No. 10/050,171**

substrate;

    a first intra-layer insulating film made of insulating material and formed on the first interlayer insulating film, the first intra-layer insulating film being formed with a recess reaching a bottom of the first intra-layer insulating film, the recess having a pad part and a wiring part continuous with the pad part, the pad part having a width wider than a width of the wiring part,

    a plurality of insulating regions disposed on the bottom of the pad part, and the recess being formed so that the insulating regions are not disposed in a near wiring area superposed upon an extended area of the wiring part into the pad part, within a first frame area having as an outer periphery an outer periphery of the pad part and having a first width but disposed in a second frame area having as an outer periphery an inner periphery of the first frame area and having a second width;

    a first pad filled in the pad part of the recess; and

    a wiring filled in the wiring part of the recess,

    wherein upper surfaces of said first pad, said wiring and said insulating regions are on a same level,

    wherein said first pad contained in said pad part of said recess has a continuous body,

    wherein the insulating regions are disposed regularly in the second frame area along a first direction at a first period P, and a width of the first frame area along the first direction is equal to or wider than said first period P,

    wherein said first period P is a distance from one insulating region to another insulating

region of said plurality of insulating regions including a width of said one insulating region.

**Claim 10 (Previously Presented):** A semiconductor device according to claim 9, wherein the insulating regions are not disposed in a central area on an inner side of the second frame area.

**Claim 11 (Previously Presented):** A semiconductor device according to claim 8, wherein the via hole are included in the first pad as viewed along a direction parallel to a substrate normal.

**Claim 12 (Canceled):**

**Claim 13 (Previously Presented):** A semiconductor device according to claim 8, further comprising a conductive wire wire-bonded to the second pad, wherein the insulating regions are not disposed in a central area on an inner side of the second frame area, the via hole are disposed in the central area, and a contact area between the conductive wire and the second pad extends to an area on an outer side of the via hole as viewed along a direction parallel to a substrate normal.

**Claims 14 -19 (Canceled).**

**Claim 20 (Previously Presented):** A semiconductor device according to claim 9, wherein a bottom of the recess formed in the first intra-layer insulating film is defined by the first interlayer

insulating film.

**Claim 21 (Currently Amended):** A semiconductor device comprising:

a semiconductor substrate;

a first interlayer insulating film made of insulating material and formed on the semiconductor substrate;

a first intra-layer insulating film made of insulating material and formed on the first interlayer insulating film, the first intra-layer insulating film being formed with a recess reaching a bottom of the first intra-layer insulating film, the recess having a pad part and a wiring part continuous with the pad part, the pad part having a width wider than a width of the wiring part,

a plurality of insulating regions disposed on the bottom of the pad part, and the recess being formed so that the insulating regions are not disposed in a near wiring area superposed upon an extended area of the wiring part into the pad part, within a first frame area having as an outer periphery an outer periphery of the pad part and having a first width but disposed in a second frame area having as an outer periphery an inner periphery of the first frame area and having a second width;

a first pad filled in the pad part of the recess; and

a wiring filled in the wiring part of the recess,

wherein upper surfaces of said first pad, said wiring and said insulating regions are on a same level,

**Preliminary Amendment filed June 8, 2007  
U.S. Patent Application Serial No. 10/050,171**

wherein the wiring width W1 is in a range from 5  $\mu\text{m}$  to 10  $\mu\text{m}$ , and L1/W1 is 35% or higher, wherein W1 corresponds to the width of said wiring part, L1 corresponds to the width of said first width.

**Claim 22 (Currently Amended):** A semiconductor device comprising:

a semiconductor substrate;

a first interlayer insulating film made of insulating material and formed on the semiconductor substrate;

a first intra-layer insulating film made of insulating material and formed on the first interlayer insulating film, the first intra-layer insulating film being formed with a recess reaching a bottom of the first intra-layer insulating film, the recess having a pad part and a wiring part continuous with the pad part, the pad part having a width wider than a width of the wiring part,

a plurality of insulating regions disposed on the bottom of the pad part, and the recess being formed so that the insulating regions are not disposed in a near wiring area superposed upon an extended area of the wiring part into the pad part, within a first frame area having as an outer periphery an outer periphery of the pad part and having a first width but disposed in a second frame area having as an outer periphery an inner periphery of the first frame area and having a second width;

a first pad filled in the pad part of the recess; and

a wiring filled in the wiring part of the recess,

wherein upper surfaces of said first pad, said wiring and said insulating regions are on a same level,

wherein the wiring width W1 is narrower than 5  $\mu\text{m}$ , and L1/W1 is 30% or higher,

wherein W1 corresponds to the width of said wiring part, L1 corresponds to the width of said first width.

**Claim 23 (Previously Presented):** A semiconductor device comprising:

a semiconductor substrate;

a first interlayer insulating film made of insulating material and formed on the semiconductor substrate;

a first intra-layer insulating film made of insulating material and formed on the first interlayer insulating film, the first intra-layer insulating film being formed with a recess reaching a bottom of the first intra-layer insulating film, the recess having a pad part,

a plurality of insulating regions disposed on the bottom of the pad part, and the recess being formed so that the insulating regions are not disposed in a first frame area having as an outer periphery an outer periphery of the pad part and having a first width but disposed in a second frame area having as an outer periphery an inner periphery of the first frame area and having a second width; and

a first pad filled in the pad part of the recess,

wherein upper surfaces of said first pad and said insulating regions are on a same level,

**Preliminary Amendment filed June 8, 2007  
U.S. Patent Application Serial No. 10/050,171**

wherein the insulating regions are disposed regularly in the second frame area along a first direction at a first pitch, and a width of the first frame area along the first direction is equal to or wider than the first pitch.

**Claim 24 (New):** A semiconductor device according to claim 9, wherein the width of said pad part and the width of said wiring part are widths in a direction parallel to a boundary line between said pad part and said wiring part.

**Claim 25 (New):** A semiconductor device according to claim 21, wherein the width of said pad part and the width of said wiring part are widths in a direction parallel to a boundary line between said pad part and said wiring part.

**Claim 26 (New):** A semiconductor device according to claim 22, wherein the width of said pad part and the width of said wiring part are widths in a direction parallel to a boundary line between said pad part and said wiring part.

**Claim 27 (New):** A semiconductor device according to claim 9, wherein said first pad and said wiring are made of a conductive material.

**Preliminary Amendment filed June 8, 2007  
U.S. Patent Application Serial No. 10/050,171**

**Claim 28 (New):** A semiconductor device according to claim 21, wherein said first pad and said wiring are made of a conductive material.

**Claim 29 (New):** A semiconductor device according to claim 22, wherein said first pad and said wiring are made of a conductive material.

**Claim 30 (New):** A semiconductor device according to claim 22, wherein said first pad is made of a conductive material.